Subject

OB6683+OB2007+OB2613 PD Demo Board Manual

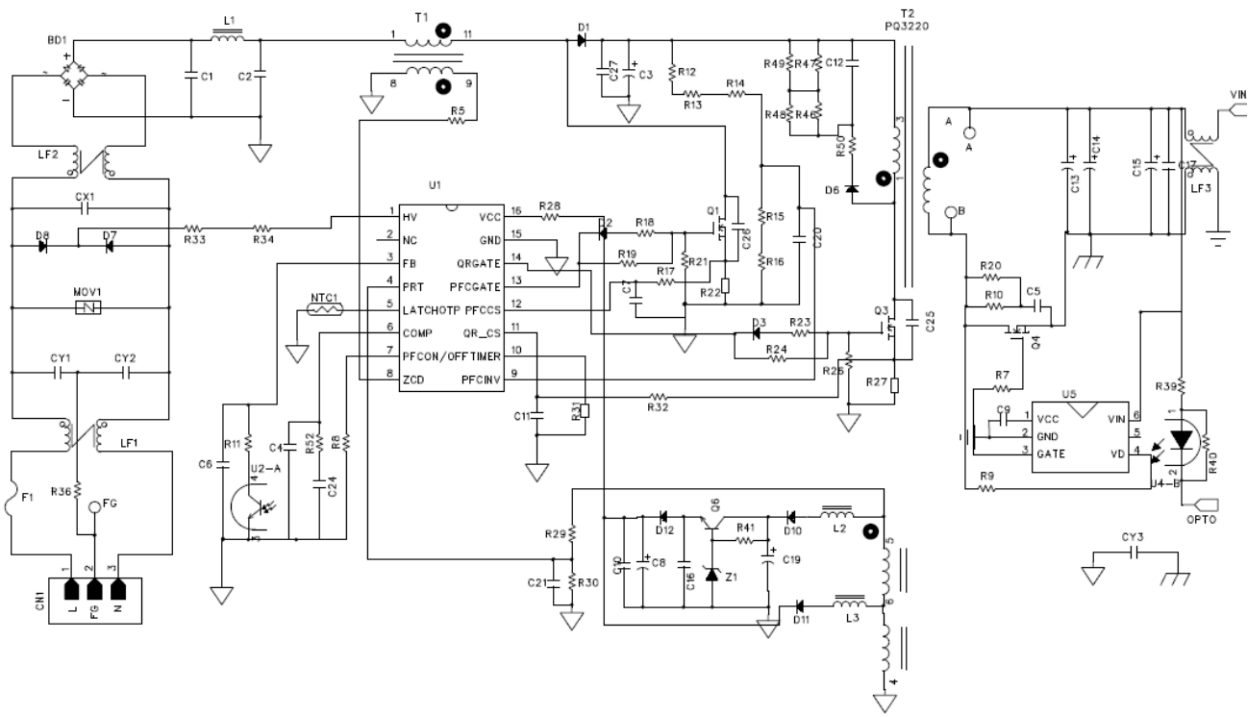
Board Model: PD20V4.5A6683_2007 1946

Doc. No.: OB_DOC_DBM_6683+2007+261301

Key features:

- Support PD3.0 protocol
- DC output:
  5V/3A,9V/3A,12V/3A,15V/3A,20V/4.5A
- PFC+QR+ Synchronous rectification for high efficiency
- Built-in dual output PFC control
- Adjustable PFC Go-to-Standby power level
- Average efficiency meet COC Ⅴ tier2
- Standby power less than 75mW @230V input
- Quick startup and enhanced dynamic response for PFC stage
- High performance Quasi-Resonant control
- Comprehensive protection coverage such as SCP、OCP、OVP、OTP
- Meet EN55032 EMI

Schematic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T1
T2
PQ3220
D1
LF2
CX1
D8
D7
MOV1
CY1
CY2
LF1
F1
FG
CN1
L
FG
N
U1
HV
NC
FB
PRT
LATCHOTP
COMP
PFCON/OFFTIMER
ZCD
VCC
GND
QRGATE
PFCGATE
PFCCS
QR_CS
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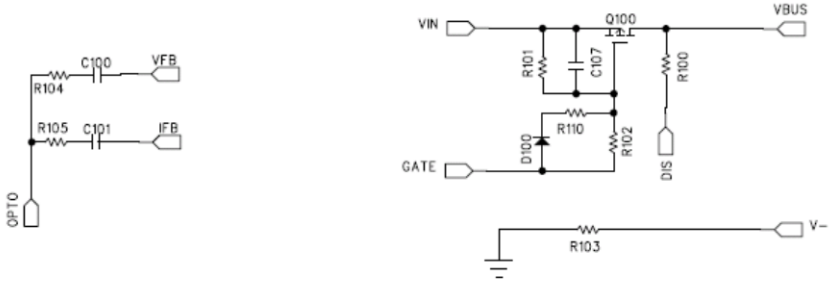
GND
GATE
VIN
VD
OPTO
LF3
CY3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R101
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R102
DIS
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R103
V-
C100
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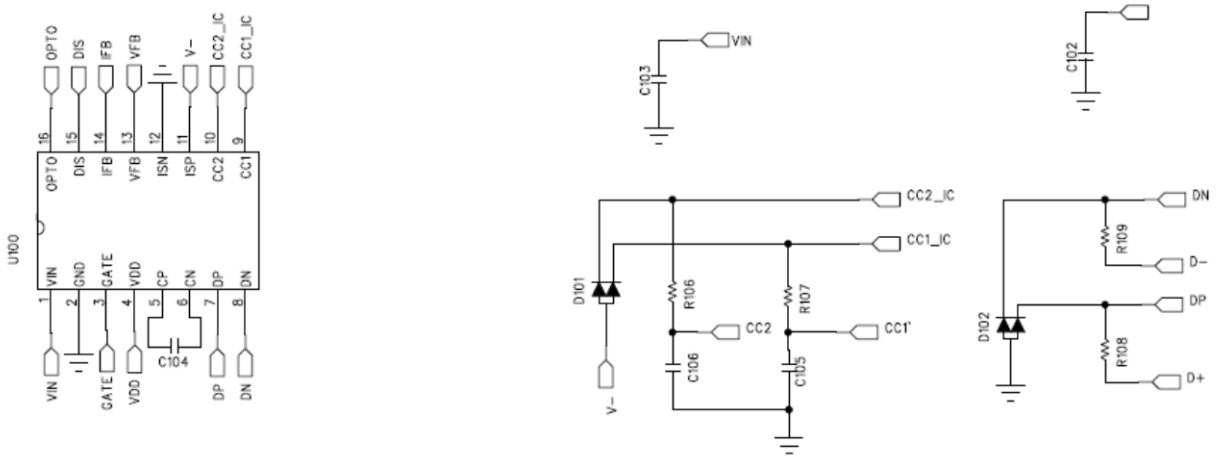
R105
C101
IFB
OPTO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CC2_IC
CC1_IC
V-
C103
VDD
C102
D101
R106
R107
CC2
CC1'
C106
C105
D102
R109
R108
D-
D+

Performance Evaluation

1. Input Characteristics

1.1 Standby Power/PF/THD

Table. 1 Standby Power(No load)

Input voltage	Standby power(mW)	Vo(V)
90Vac/60Hz	44	4.97
115Vac/60Hz	50	4.97
230Vac/50Hz	58	4.97
264Vac/50Hz	66	4.97

Table. 2 PF/THD(Full load)

Input voltage	PF	THD(%)
90Vac/60Hz	0.99	12
115Vac/60Hz	0.98	12
230Vac/50Hz	0.97	13
264Vac/50Hz	0.96	14

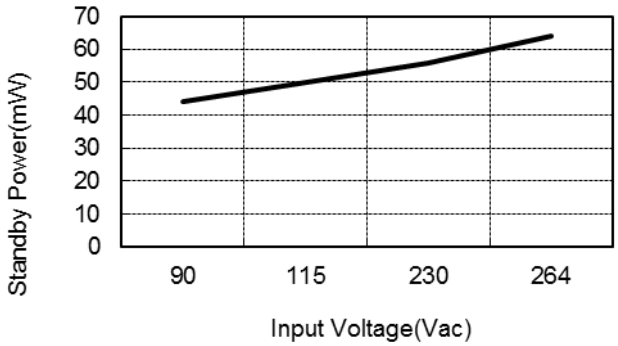


Fig. 1 No-load Input Power vs. Input Line Voltage

1.2 Efficiency

Table. 3 Efficiency@PCB End

5V3A								
	100%	75%	50%	25%	AVE	CoC Req	10%	CoC Req
115Vac	87.93%	88.12%	88.26%	87.32%	87.91%	81.84%	83.40%	72.48%
230Vac	86.95%	86.72%	85.58%	84.16%	85.85%		81.00%	

9V3A								
	100%	75%	50%	25%	AVE	CoC Req	10%	CoC Req
115Vac	90.17%	90.28%	90.44%	89.69%	90.14%	87.30%	85.72%	77.30%
230Vac	90.34%	90.09%	89.42%	87.82%	89.42%		83.23%	

12V3A								
	100%	75%	50%	25%	AVE	CoC Req	10%	CoC Req
115Vac	90.47%	90.70%	90.78%	90.36%	90.58%	88.30%	85.80%	78.30%
230Vac	91.09%	91.02%	90.61%	88.96%	90.42%		84.23%	

15V3A								
	100%	75%	50%	25%	AVE	CoC Req	10%	CoC Req
115Vac	90.82%	90.82%	91.00%	90.45%	90.77%	88.85%	88.04%	78.85%
230Vac	91.47%	91.26%	90.85%	89.36%	90.73%		84.44%	

20V4.5A								
	100%	75%	50%	25%	AVE	CoC Req	10%	CoC Req
115Vac	90.62%	91.19%	90.63%	90.75%	90.80%	89.00%	89.07%	79%
230Vac	91.35%	90.83%	91.84%	90.72%	91.19%		87.92%	

2. Output Characteristics

2.1 Line Regulation & Load Regulation

All data was measurement at @100mR CABLE end

Table 1 Line Regulation & Load Regulation

Input voltage	No load	Half load	Full load	Specification	Output Voltage
90Vac/60HZ	4.968	4.934	4.906		5V
115Vac/60HZ	4.968	4.933	4.906		
230Vac/50HZ	4.971	4.935	4.906		
264Vac/50HZ	4.971	4.934	4.905		
Line Regulation	0.06%			<2%	
Load Regulation	1.3%			<5%	

Input voltage	No load	Half load	Full load	Specification	Output Voltage
90Vac/60HZ	8.985	8.888	8.794		9V
115Vac/60HZ	8.985	8.888	8.795		
230Vac/50HZ	8.994	8.888	8.795		
264Vac/50HZ	8.985	8.886	8.794		
Line Regulation	0.1%			<2%	
Load Regulation	2.2%			<5%	

Input voltage	No load	Half load	Full load	Specification	Output Voltage
90Vac/60HZ	11.992	11.898	11.803		12V
115Vac/60HZ	11.992	11.895	11.805		
230Vac/50HZ	11.994	11.895	11.804		
264Vac/50HZ	11.99	11.895	11.803		
Line Regulation	0.03%			<2%	
Load Regulation	1.6%			<5%	

Input voltage	No load	Half load	Full load	Specification	Output Voltage
90Vac/60HZ	14.997	14.903	14.815		15V
115Vac/60HZ	14.998	14.905	14.816		
230Vac/50HZ	14.997	14.905	14.815		
264Vac/50HZ	14.996	14.904	14.813		
Line Regulation	0.02%			<2%	
Load Regulation	1.2%			<5%	

Input voltage	No load	Half load	Full load	Specification	Output Voltage
90Vac/60HZ	20.007	19.852	19.708		20V
115Vac/60HZ	20.006	19.854	19.710		
230Vac/50HZ	20.007	19.854	19.710		
264Vac/50HZ	20.007	19.854	19.712		
Line Regulation	0.02%			<2%	
Load Regulation	1.5%			<5%	

2.2 Ripple & Noise

All data was measurement at @100mR CABLE end

Table 2 Ripple & Noise

Input voltage	5V R&N (mV)

	No load	Full load	Remark
90Vac/60HZ	73mv	110mv	Fig 2-5
264Vac/50HZ	66mv	103mv	

Input voltage	9V R&N (mV)		
	No load	Full load	Remark
90Vac/60HZ	72mv	125mv	
264Vac/50HZ	60mv	100mv	

Input voltage	12V R&N (mV)		
	No load	Full load	Remark
90Vac/60HZ	67mv	128mv	
264Vac/50HZ	60mv	100mv	

Input voltage	15V R&N (mV)		
	No load	Full load	Remark
90Vac/60HZ	69mv	134mv	
264Vac/50HZ	63mv	120mv	

Input voltage	20V R&N (mV)		
	No load	Full load	Remark
90Vac/60HZ	63mv	195mv	Fig 6-9
264Vac/50HZ	66mv	166mv	

Note: Ripple& noise was measured at DC cord end without probe cap and ground clip. Measurement bandwidth was limited to 20MHZ.

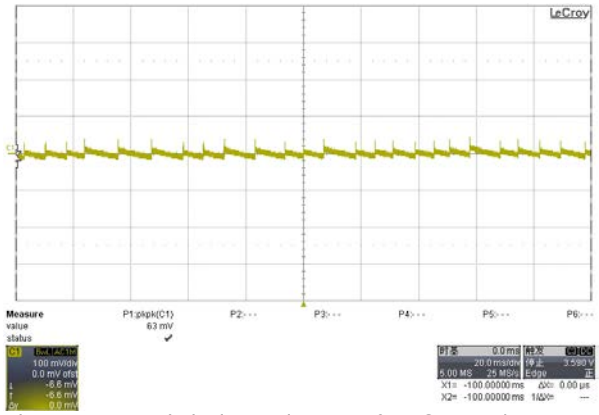


Fig. 2 Measured ripple& noise waveform@90Vac/60HZ, no load.

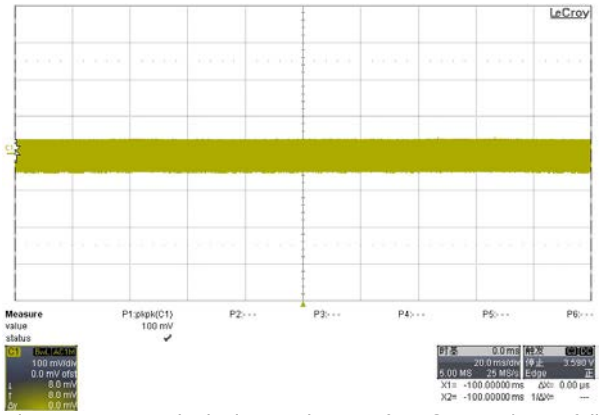


Fig. 3 Measured ripple& noisewaveform@90Vac/60HZ,full load.

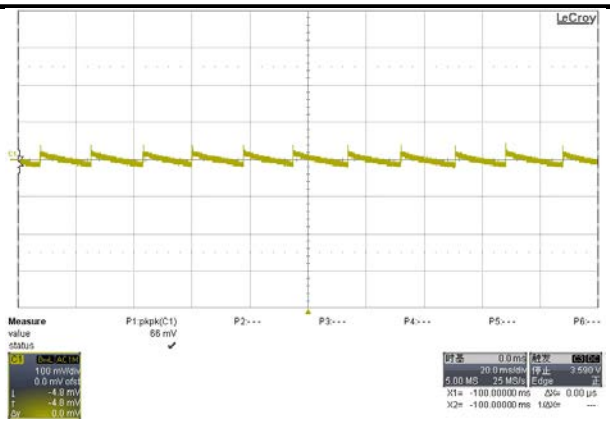


Fig. 4 R&N waveform@264Vac; no load

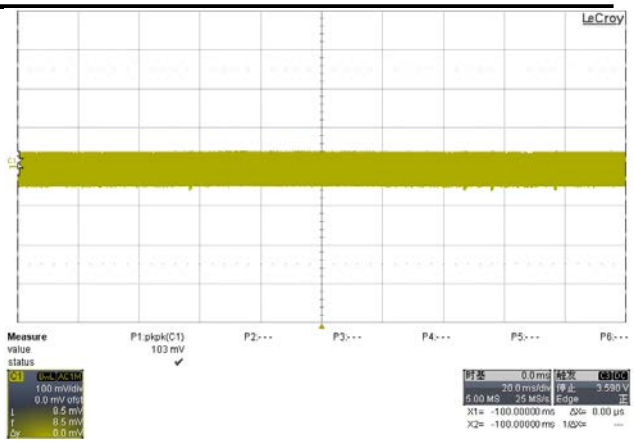


Fig. 5 R&N waveform@264Vac; full load

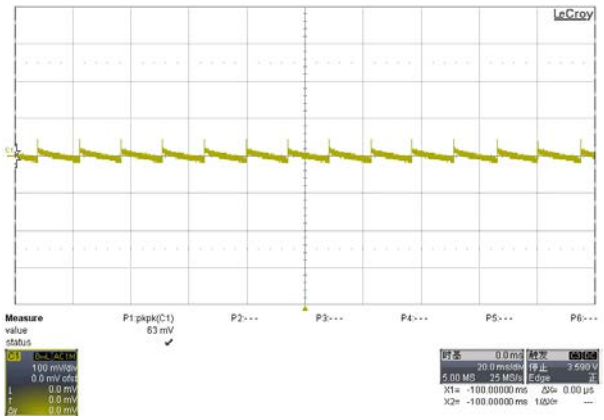


Fig. 6 Measured ripple& noise waveform@90Vac/60HZ, no load.

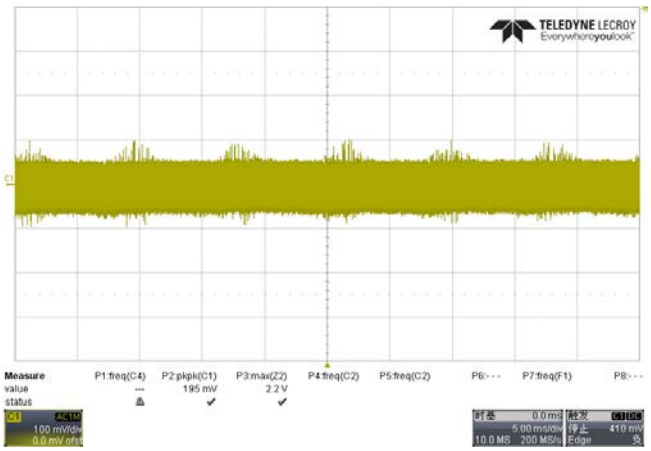


Fig. 7 Measured ripple& noisewaveform@90Vac/60HZ,full load.

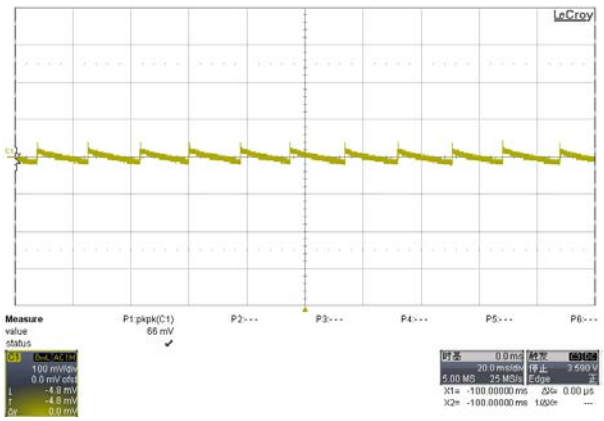


Fig. 8 R&N waveform@264Vac; no load

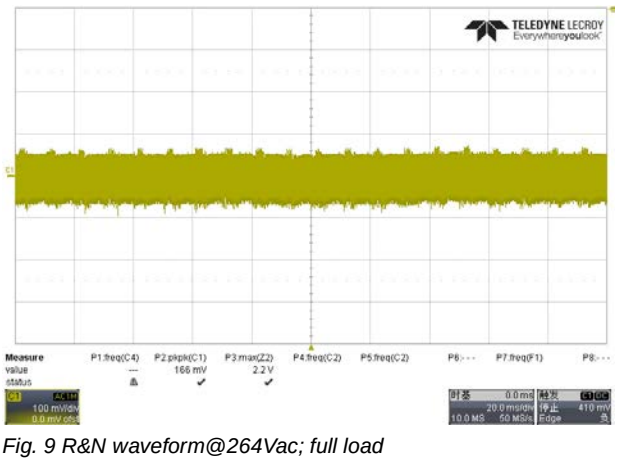


Fig. 9 R&N waveform@264Vac; full load

2.3 Dynamic Test

A dynamic loading with low set at 10% full load lasting for 10mS and high set at 90% full load lasting for 10mS is added to output. The ramp is set at 0.25A/uS at transient.
All data was measurement at @100mR CABLE end.

Table 3 Output voltage under dynamic test

Input voltage	5V Output voltage (mV)	Waveform

90V/60HZ	±415	Fig.16-17
264V/50HZ	±432	

Input voltage	9V Output voltage (mV)	Waveform
90V/60HZ	±415	
264V/50HZ	±432	

Input voltage	12V Output voltage (mV)	Waveform
90V/60HZ	±415	
264V/50HZ	±432	

Input voltage	15V Output voltage (mV)	Waveform
90V/60HZ	±415	
264V/50HZ	±432	

Input voltage	20V Output voltage (mV)	Waveform
90V/60HZ	±600	Fig.18-19
264V/50HZ	±615	

Dynamic waveform

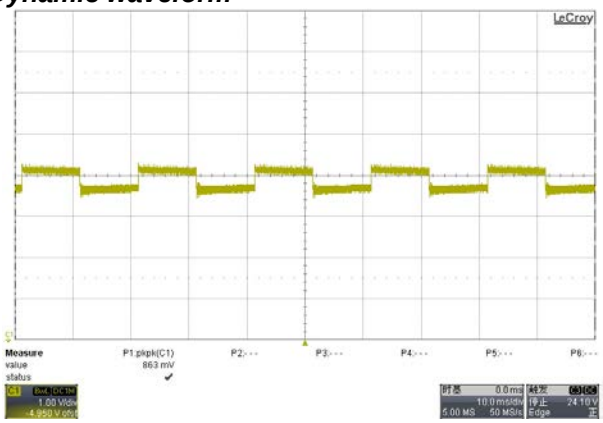


Fig. 10 Dynamic waveform@90Vac input

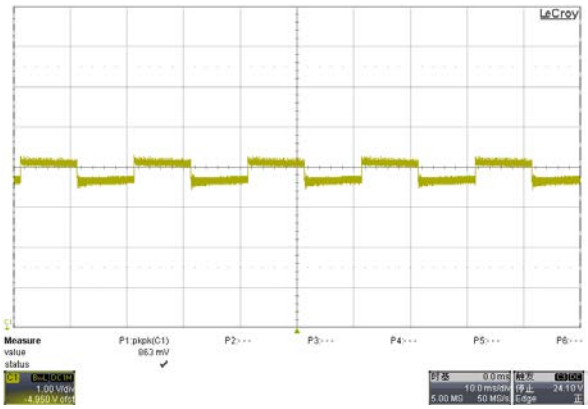


Fig. 11 Dynamic waveform@264Vac input

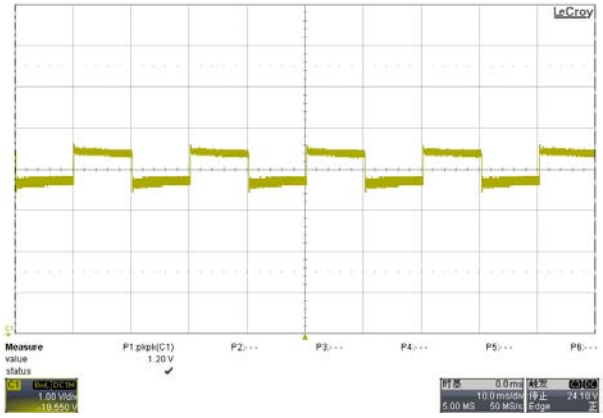


Fig. 12 Dynamic waveform@90Vac input

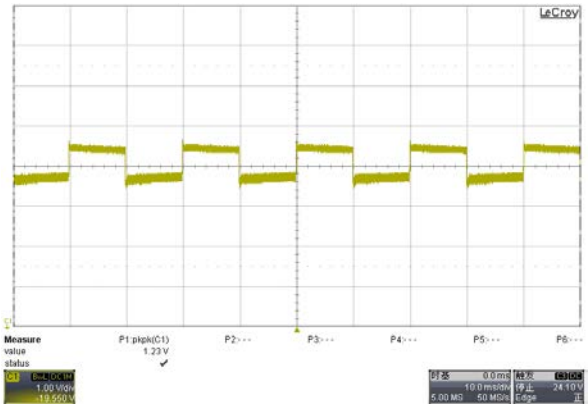
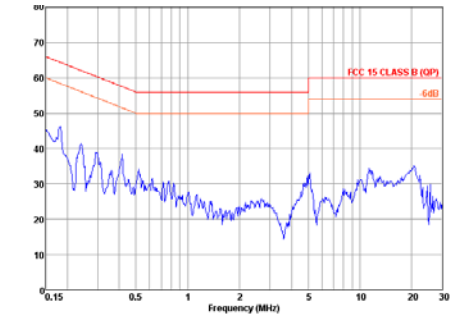


Fig. 13 Dynamic waveform@264Vac input

3. EMI Test

The Power supply passed EN55032 Class B & FCC class B EMI requirement with more than 6dB margin

3.1 Conducted EMI Test

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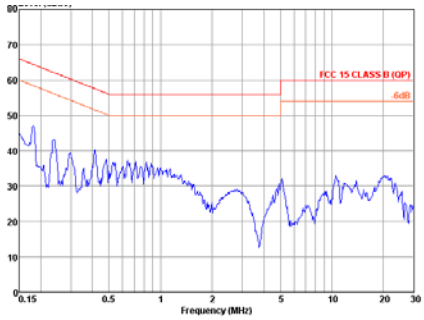
Site          : Audix (Shanghai) Shielded 3
Condition     : FCC 15 CLASS B (QP) ENV4200-2019 NEUTRAL
Project No.   :
Applicant     :
EUT           : OB6683 PD90W
M/N           : 20V 4.5A
S/N           :
Power Supply  : 120V/60Hz
Ambient       : 23'C/52%RH
Test Line     : N
Test Mode     :
Test Engineer: Kevin
Memo          :
```

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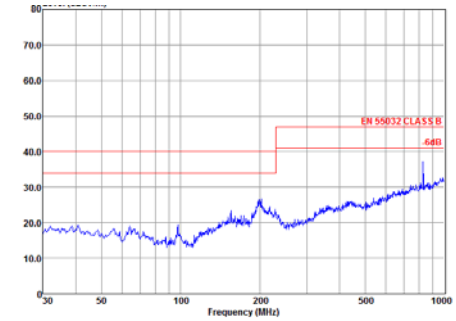
Condition     : FCC 15 CLASS B (QP) ENV4200-2019 LINE
Project No.   :
Applicant     :
EUT           : OB6683 PD90W
M/N           : 20V 4.5A
S/N           :
Power Supply  : 120V/60Hz
Ambient       : 23'C/52%RH
Test Line     : L
Test Mode     :
Test Engineer: Kevin
Memo          :
```

3.2 Radiation EMI Test

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Condition     : EN 55032 CLASS B HORIZONTAL
Project No.   :
Applicant     :
EUT           :
M/N           : OB6683PD90W
S/N           :
Power Supply  : 230V/50Hz
Ambient       : 22'C  60%RH
Test Mode     : 20V 4.5A
Test Engineer: Richard
Memo          :
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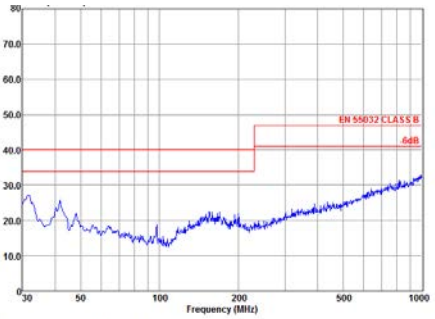


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Condition     : EN 55032 CLASS B VERTICAL
Project No.   :
Applicant     :
EUT           :
M/N           : OB6683PD90W
S/N           :
Power Supply  : 230V/50Hz
Ambient       : 22'C  60%RH
Test Mode     : 20V 4.5A
Test Engineer: Richard
Memo          :
```

4. PD Specification Test

4.1 Vbus Change Test

Vbus changing test between 5V/9V/12V/15V/20V under No load/Full load conditions

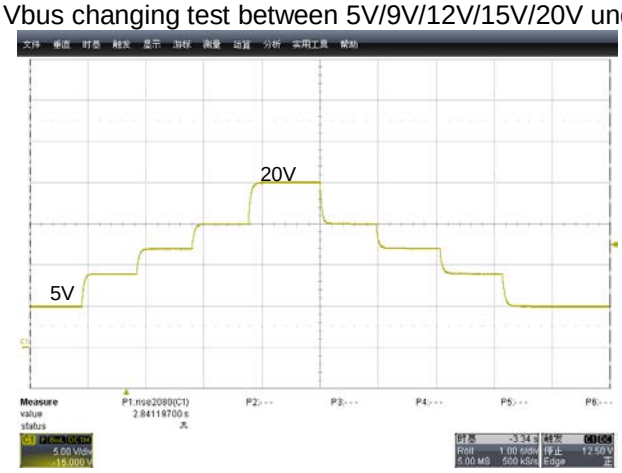

Fig. 14 Vbus Changing Test @no load

Fig. 15 Vbus Changing Test @full load

4.2 Negative Voltage Transitions

Vbus changing test from 20V to 5V @No load/Full load. The transition time is 167ms（spec: <275ms）

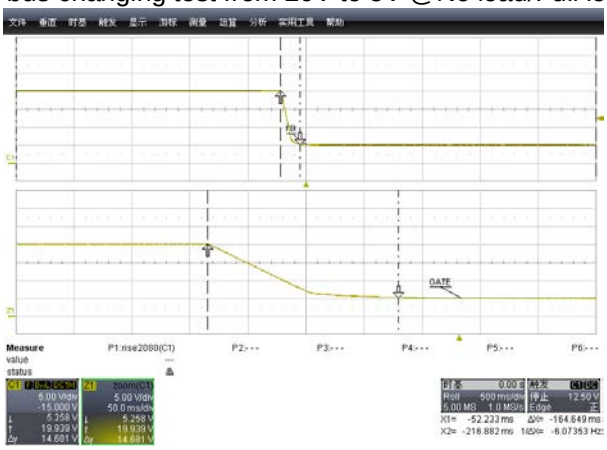

Fig. 16 Vbus Change From 20V to 5V @no load

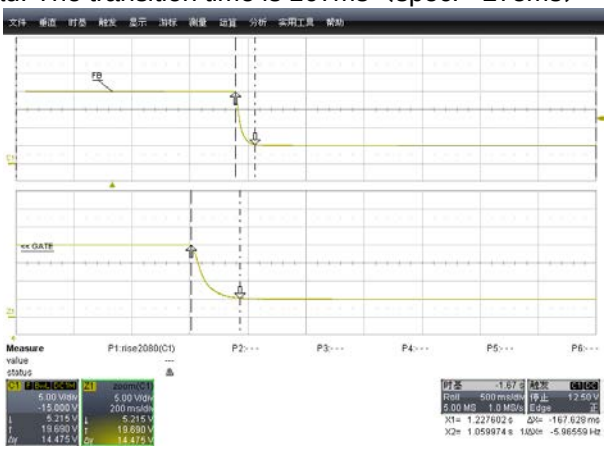

Fig. 17 Vbus Change From 20V to 5V @full load

4.3 Positive Voltage Transitions

Vbus changing test from 5V to 20V @No load/Full load. The transition time is 140ms（spec: <275ms）

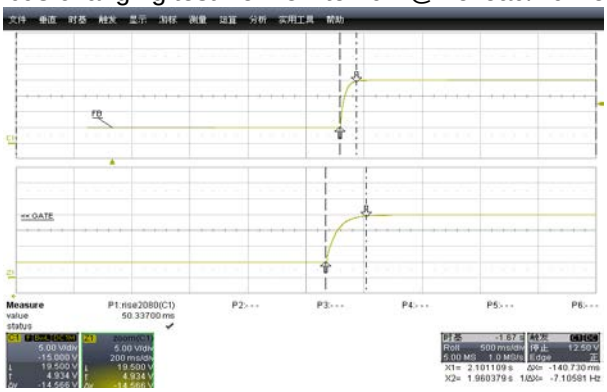

Fig. 18 Vbus Change From 5V to 20V @no load

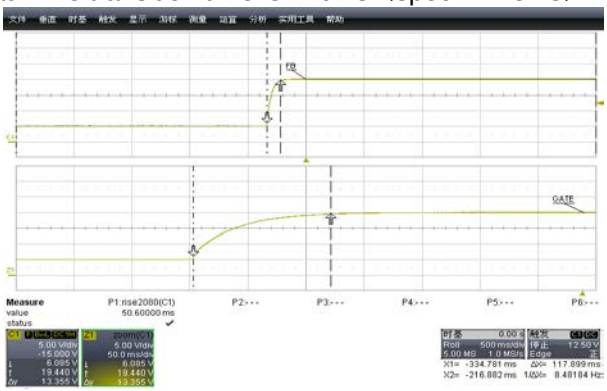

Fig. 19 Vbus Change From 5V to 20V @full load

4.4 Response to Hard Resets

When responding to hard reset, the time of tSafe5V/tSafe0V/tSrcRecover/tSrcTurnon are strict following PD spec.

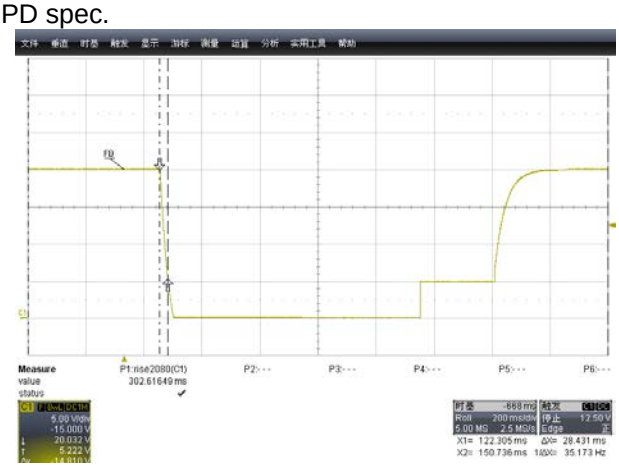

Fig. 20 Hard Reset t0-tSafe5V（spec: <275ms）

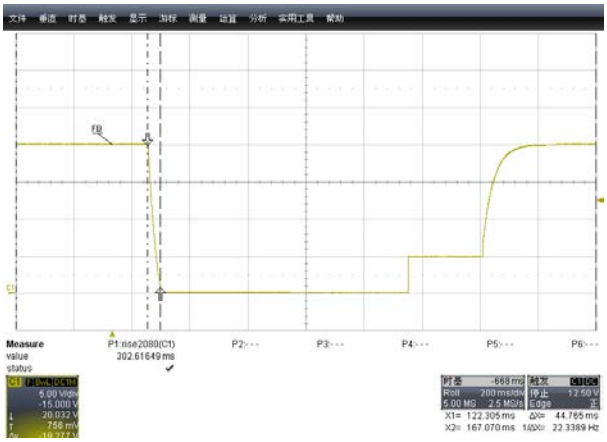

Fig. 21 Hard Reset t0-tSafe0V（spec: <650ms）

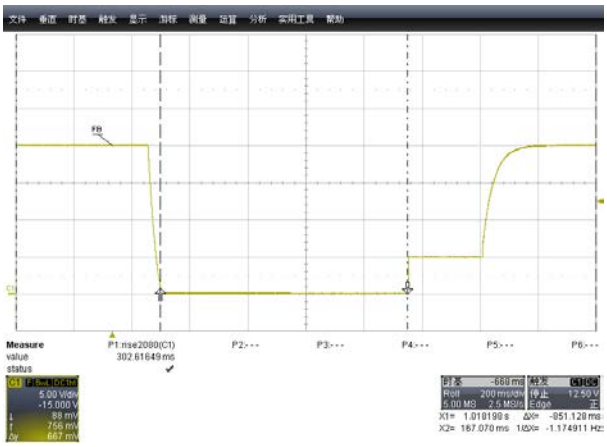

Fig. 22 Hard Reset tSrcRecover（660ms<spec<1s）

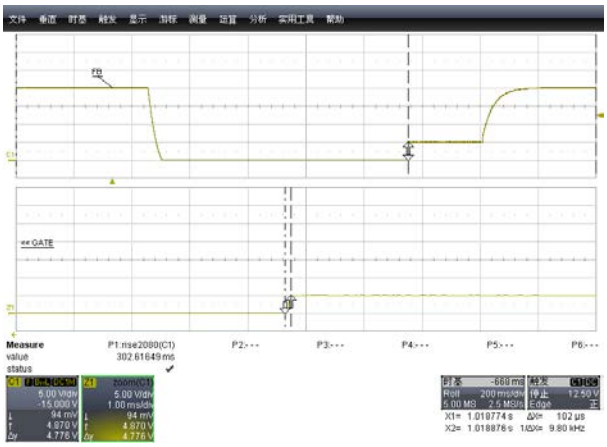

Fig. 23 Hard Reset tSrcTurnon（spec: <275ms）

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