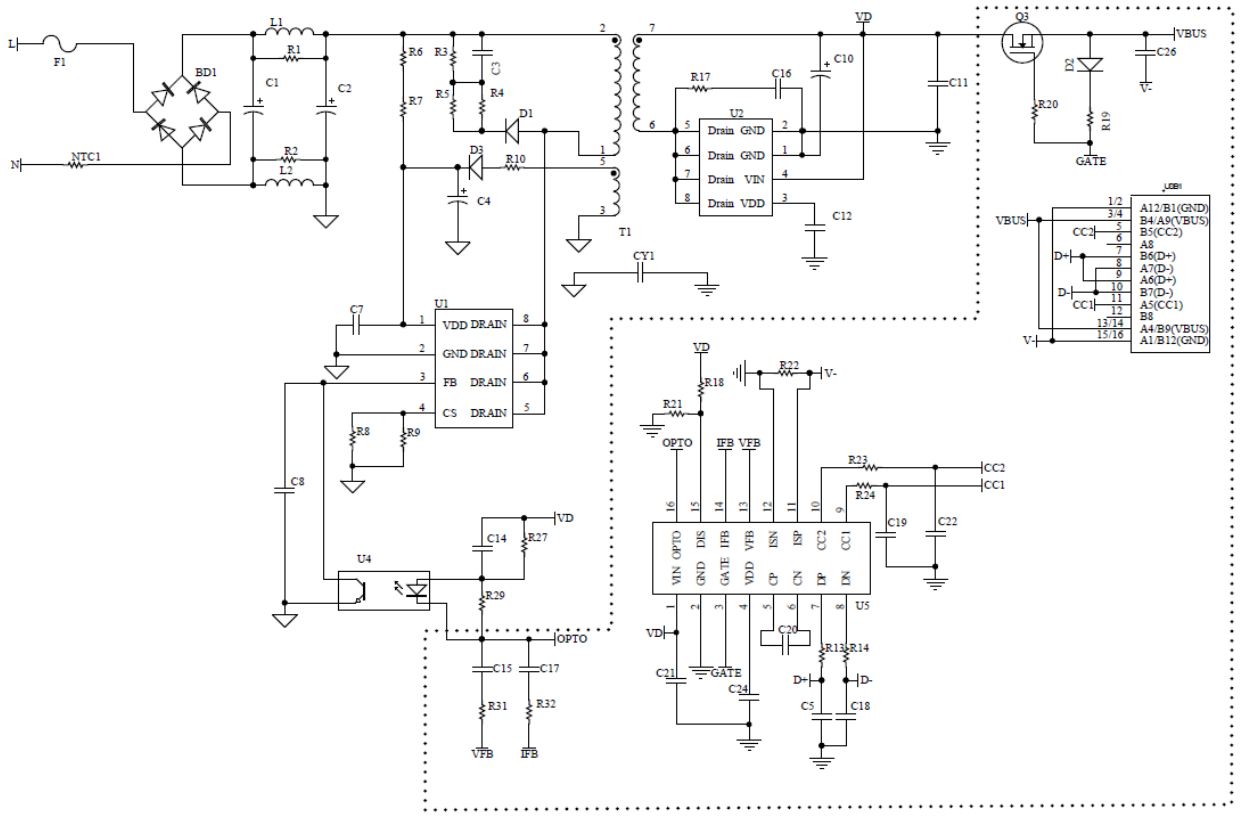
Subject	
OB2631U+OB2613 Demo Board Manual	Board Model: PD20W OB2631U+OB2613N

Key features:

- Support PD3.0 protocol@ Include PPS
- Support QC4/QC3/QC2/FCP/SCP/Apple/ Samsung/BC1.2
- SSR+ Synchronous rectification for high efficiency
- DC output: 5V/3A , 9V/2.22A , 12V/1.67A
- Standby power less than 75mW @264Vac
- Average efficiency meet DOE &COC
- Comprehensive protection coverage with auto-recovery, such as OCP、OVP、OTP etc.
- Meet EN55032 Class B & FCC CLASS B EMI

Schematic



Performance Evaluation

1. Input Characteristics

1.1 Standby power

Table 1 Standby power at no load

Input voltage	Pin(mW)	Vo(V)	Specification	Test result
100Vac/60HZ	28	5.05	<75mW	**Pass**
115Vac/60HZ	31	5.05		
230Vac/50HZ	57	5.05		
264Vac/50HZ	68	5.05		

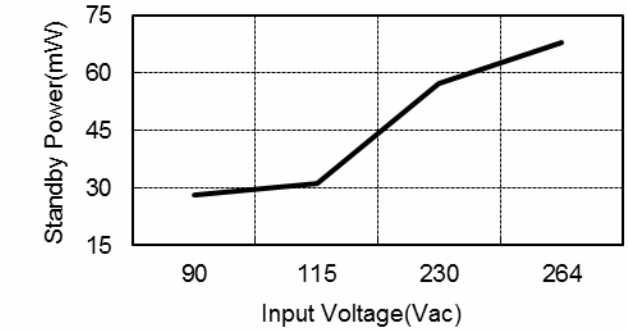


Fig. 1 No-load Input Power vs. Input Line Voltage (5V

1.2 Efficiency

Table 1 Efficiency @PCB End

5V3A								
	100%	75%	50%	25%	AVE	CoC Req	10%	CoC Req
115Vac	88.12%	89.1%	89.83%	90.51%	89.39%	81.84%	88.00%	72.48%
230Vac	88.61%	88.78%	89.21%	89.27%	89.03%		84.02%	

9V2.22A								
	100%	75%	50%	25%	AVE	CoC Req	10%	CoC Req
115Vac	89.45%	90.13%	90.73%	91.14%	90.36%	85.96%	87.11%	75.96%
230Vac	90.34%	90.34%	90.4%	90.29%	90.34%		84.36%	

12V1.67A								
	100%	75%	50%	25%	AVE	CoC Req	10%	CoC Req
115Vac	89.96%	90.66%	90.93%	91.10%	90.66%	85.98%	84.73%	75.98%
230Vac	90.87%	90.88%	90.6%	90.18%	90.63%		82.16%	

2. Output Characteristics

2.1 Line Regulation & Load Regulation

All data was measurement at @100mR CABLE end

Table 2 Line Regulation & Load Regulation

Input voltage	No load	Half load	Full load	Specification	Output Voltage
100Vac/60HZ	4.970	4.945	4.932		5V
115Vac/60HZ	4.970	4.945	4.932		
230Vac/50HZ	4.971	4.945	4.932		
264Vac/50HZ	4.972	4.945	4.932		
Line Regulation	±0.01%			<2%	
Load Regulation	±0.03%			<5%	

Input voltage	No load	Half load	Full load	Specification	Output Voltage
100Vac/60HZ	9.019	8.956	8.896		9V
115Vac/60HZ	9.019	8.956	8.896		
230Vac/50HZ	9.019	8.956	8.896		
264Vac/50HZ	9.019	8.956	8.896		
Line Regulation	±0.01%			<2%	
Load Regulation	±0.05%			<5%	

Input voltage	No load	Half load	Full load	Specification	Output Voltage
100Vac/60HZ	12.045	11.998	11.955		12V
115Vac/60HZ	12.045	11.998	11.955		
230Vac/50HZ	12.045	11.998	11.955		
264Vac/50HZ	12.045	11.998	11.955		
Line Regulation	±0.004%			<2%	
Load Regulation	±0.02%			<5%	

2.2 Ripple & Noise

All data was measurement at @100mR CABLE end

Table 3 Ripple & Noise

Input voltage	5V R&N (mV)		
	No load	Full load	Remark
100Vac/60HZ	49mv	134mv	
264Vac/50HZ	77mv	127mv	

Input voltage	9V R&N (mV)		
	No load	Full load	Remark
100Vac/60HZ	79mv	132mv	
264Vac/50HZ	75mv	154mv	

Input voltage	12V R&N (mV)		
	No load	Full load	Remark
100Vac/60HZ	79mv	147mv	
264Vac/50HZ	75mv	134mv	

Note: Ripple& noise was measured at DC cord end without probe cap and ground clip. Measurement bandwidth was limited to 20MHZ.

2.3 Dynamic Test

A dynamic loading with low set at 10% full load lasting for 10mS and high set at 90% full load lasting for 10mS is added to output. The ramp is set at 0.25A/uS at transient.
All data was measurement at @100mR CABLE end.

Table 4 Output voltage under dynamic test

Input voltage	5V Output voltage (V)	Waveform
100V/60HZ	5.21V-4.51V	Fig.15-16
264V/50HZ	5.21V-4.52V	

Input voltage	9V Output voltage (V)	Waveform
100V/60HZ	9.12V-8.62V	
264V/50HZ	9.12V-8.59V	

Input voltage	12V Output voltage (V)	Waveform
100V/60HZ	12.02V-11.58V	Fig.17-18
264V/50HZ	12.02V-11.58V	

Dynamic waveform

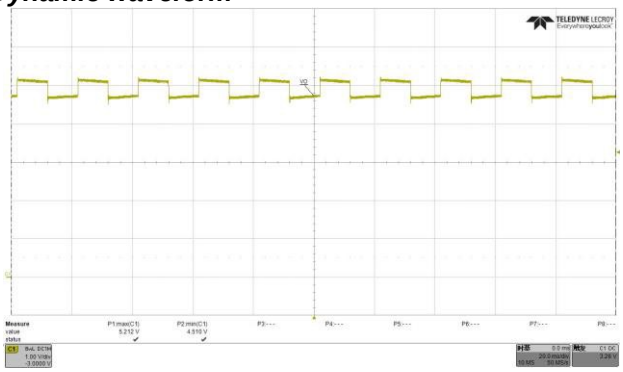


Fig. 1 Dynamic waveform@100Vac input

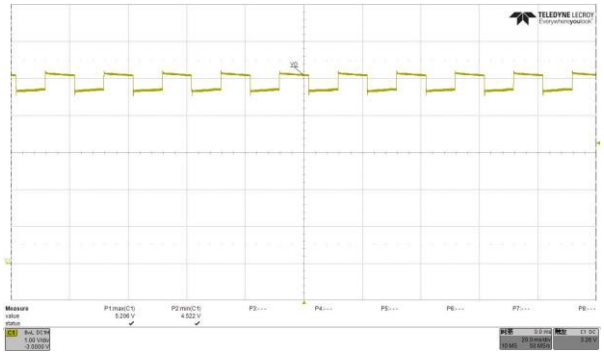


Fig. 2 Dynamic waveform@264Vac input

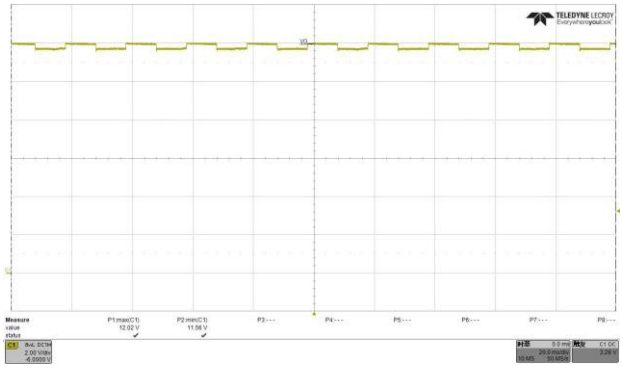


Fig. 3 Dynamic waveform@100Vac input

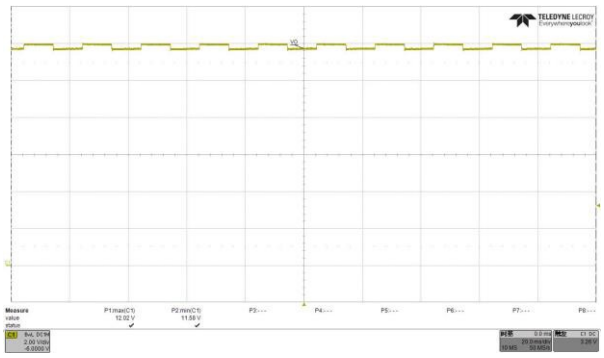
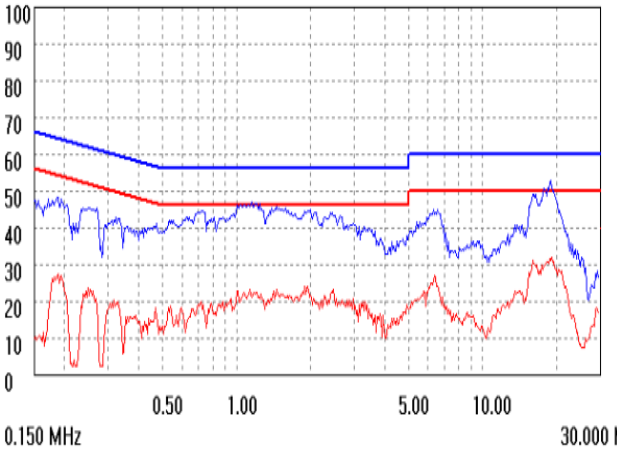


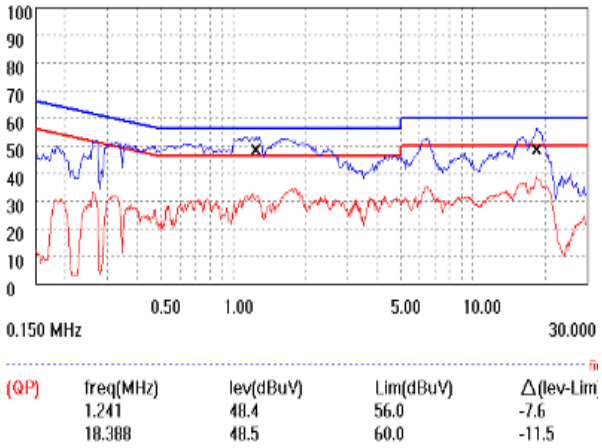
Fig. 4 Dynamic waveform@264Vac input

3. EMI Test

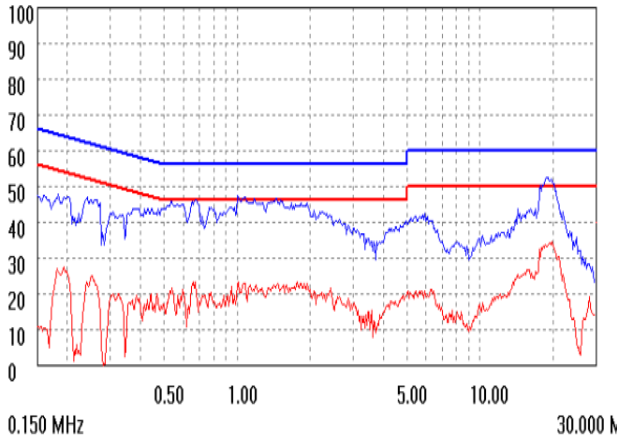
The Power supply passed EN55022 Class B & FCC class B EMI requirement with more than 6dB margin tested with shield。



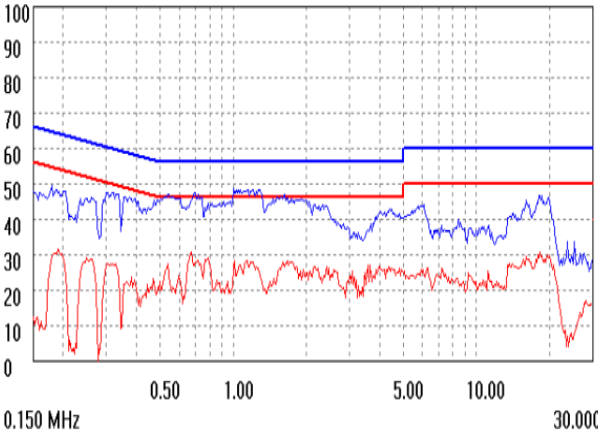
5V3A L



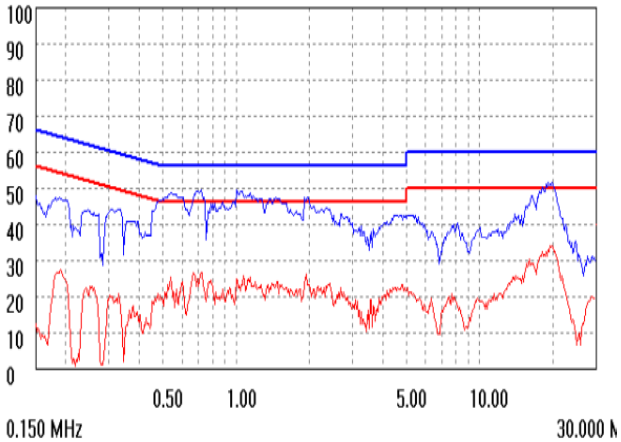
5V3A N



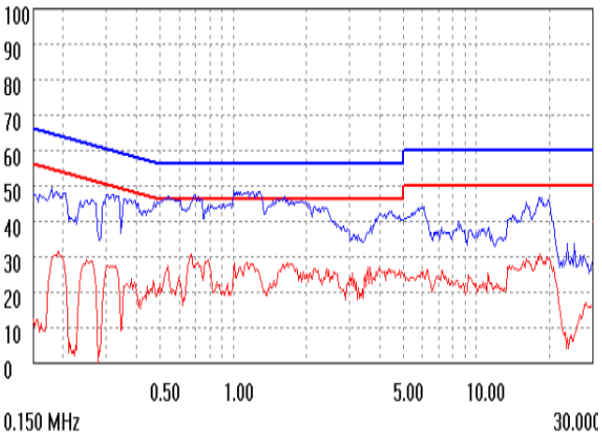
9V2.22A L



9V2.22A N



12V1.67A L



12V1.67A N

4. PD Specification Test

4.1 Vbus Change Test

Vbus changing test between 5V/9V/12V

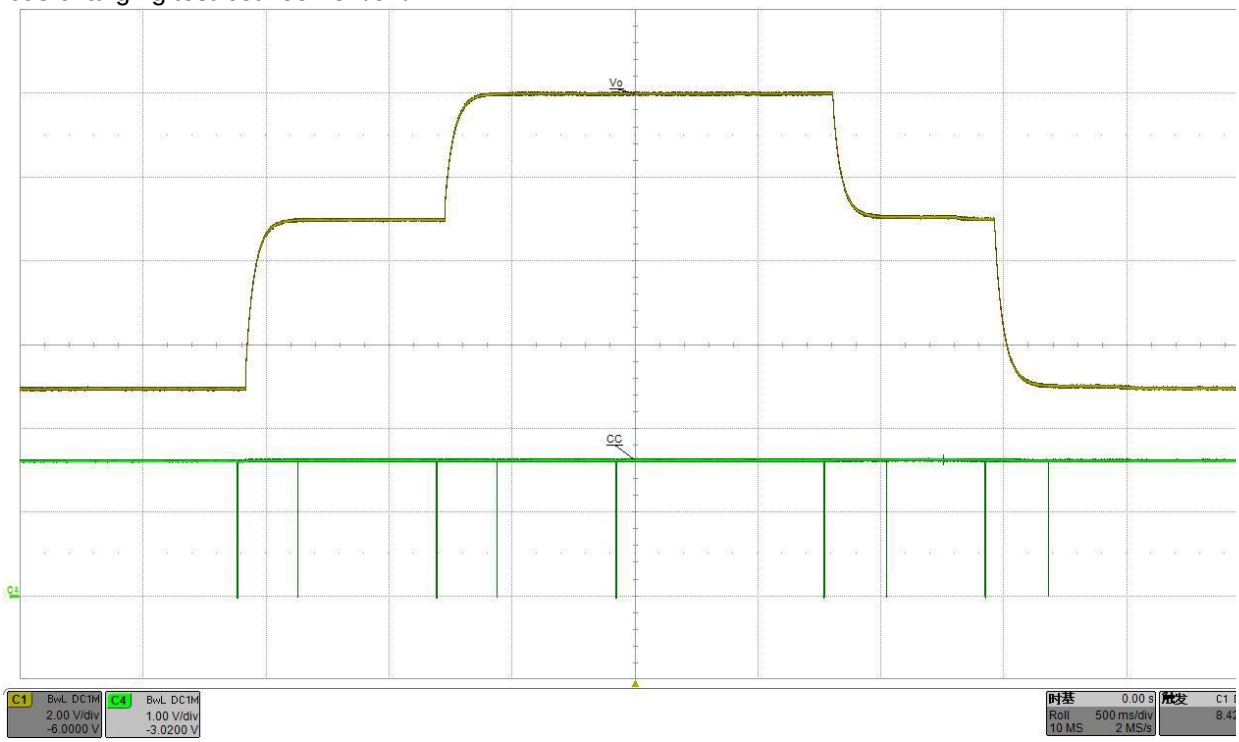


Fig. 5 Vbus Changing Test @no load

4.2 Negative Voltage Transitions

Vbus changing test from 12V to 5V @No load/Full load. The transition time is 126ms（spec: <275ms）

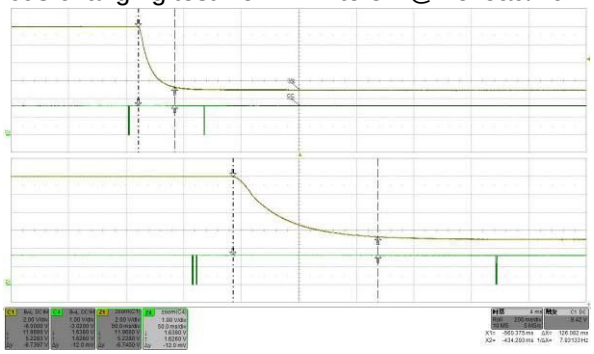


Fig. 42 Vbus Change From 12V to 5V @no load

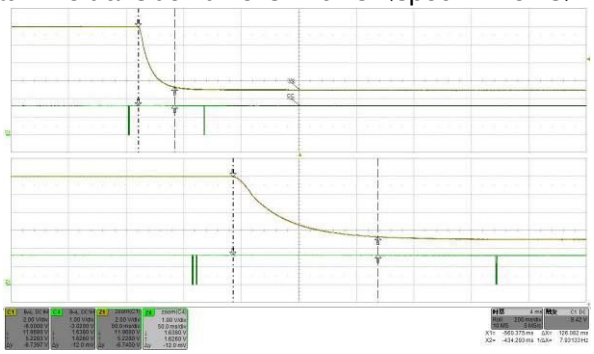


Fig. 6 Vbus Change From 12V to 5V @full load

4.3 Positive Voltage Transitions

Vbus changing test from 5V to 12V @No load/Full load. The transition time is 102ms（spec: <275ms）

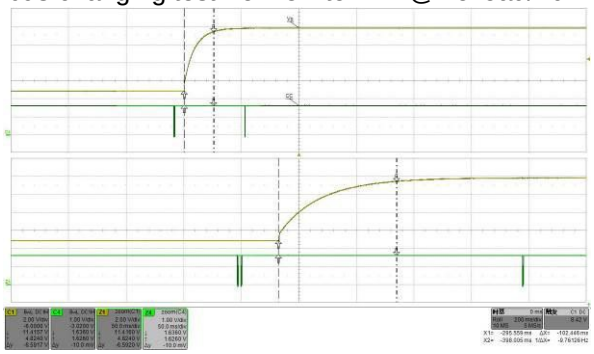


Fig. 7 Vbus Change From 5V to 12V @no load

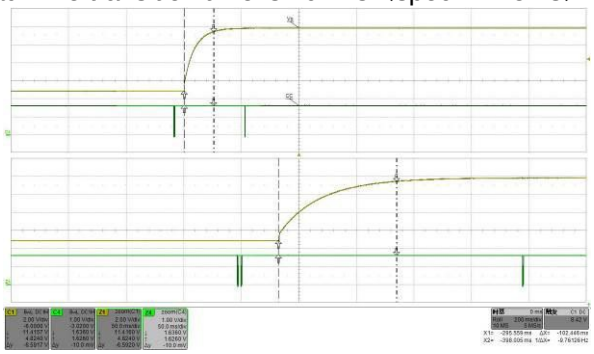


Fig. 8 Vbus Change From 5V to 12V @full load

4.4 Response to Hard Resets

When responding to hard reset, the time of tSafe5V/tSafe0V/tSrcRecover/tSrcTurnon are strict following PD spec.

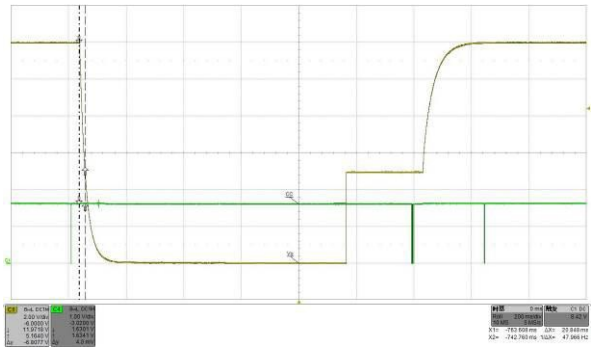


Fig. 9 Hard Reset t0-tSafe5V（spec: <275ms）

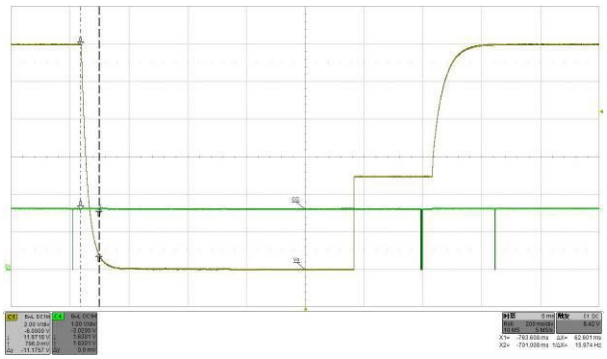


Fig. 10 Hard Reset t0-tSafe0V（spec: <650ms）

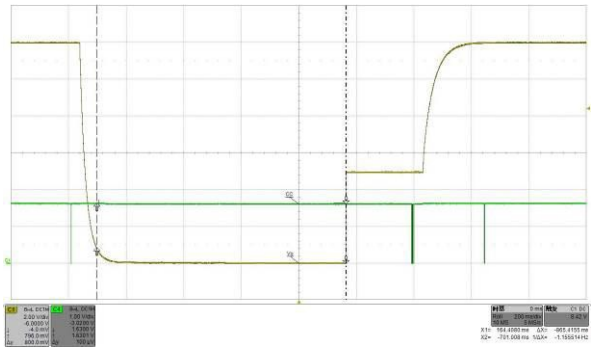


Fig. 11 Hard Reset tSrcRecover（660ms<spec<1s）

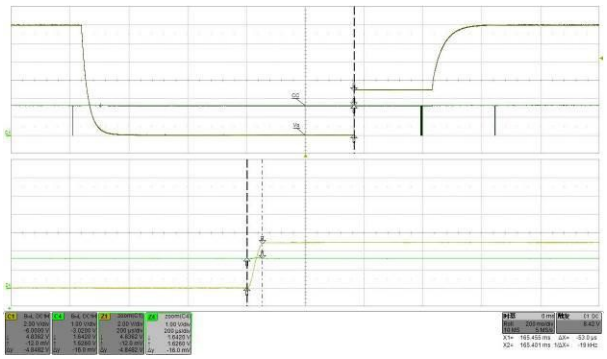


Fig. 12 Hard Reset tSrcTurnon（spec: <275ms）

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