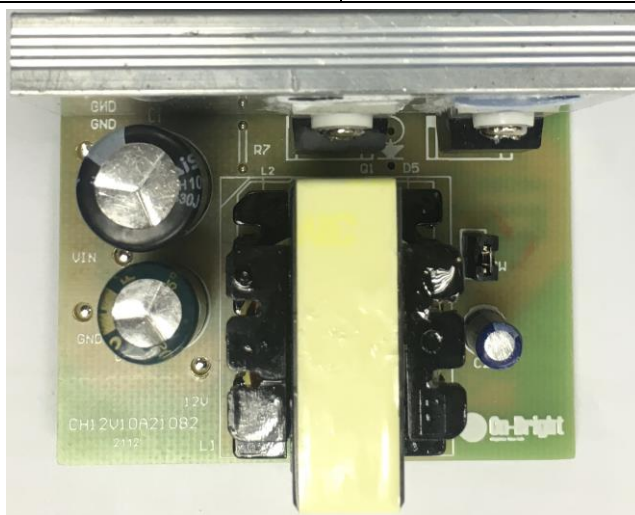


Subject

OB21082CFP Demo Board Manual

Board Model: CH12V10A21082 2112

Doc. No.: OB_DOC_DBM_A_2108200



Key features:

- Synchronous driver to achieve high efficiency
- Lowest component counts
- Precise line /load regulation (<1%)
- Adjustable OCP point
- Comprehensive protection coverage: OCP/OVP /SCP/VIN OVP&UVP/OTP
- Enable/disable function
- Shutdown delay

Revision History

Revise Date	Version	Reason/Issue
2021-03-22	00	First issue

1. Specification

1.1. Input Characteristics

- DC input voltage range 25Vdc ~ 118Vdc(36V~96V battery pack)

1.2. Output Characteristics

- Output Voltage 12.25V
- Min. load current 0mA
- Max. load current 10A

1.3. Performance Specifications

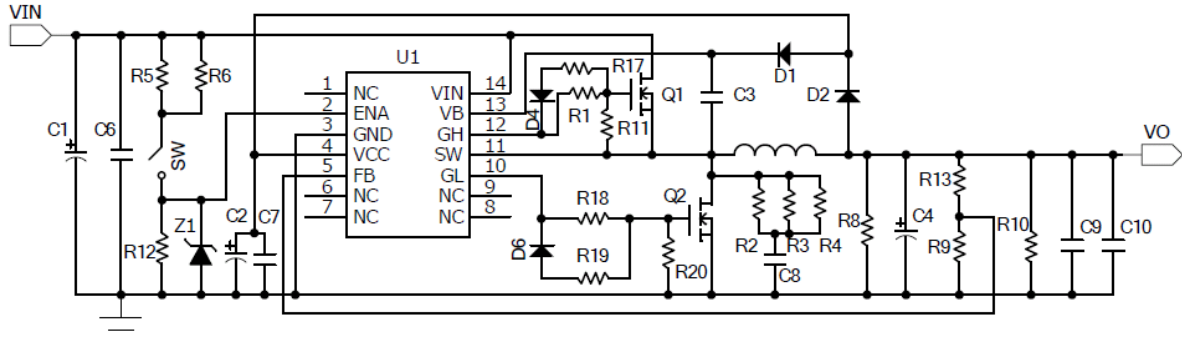
- Efficiency >91% @ 50%/100% Load, normal line,25°C
- Line Regulation 1% Max
- Load Regulation 1% Max
- Ripple & Noise 300 mV Max

1.4. Protection Features

- Vin OVP/UVP Protection Output shut down with automatic recovery
- Short circuit Protection Output shut down with latch
- Over Current Protection Output shut down with latch
- Over Temperature Protection Output shut down with automatic recovery

2. Information

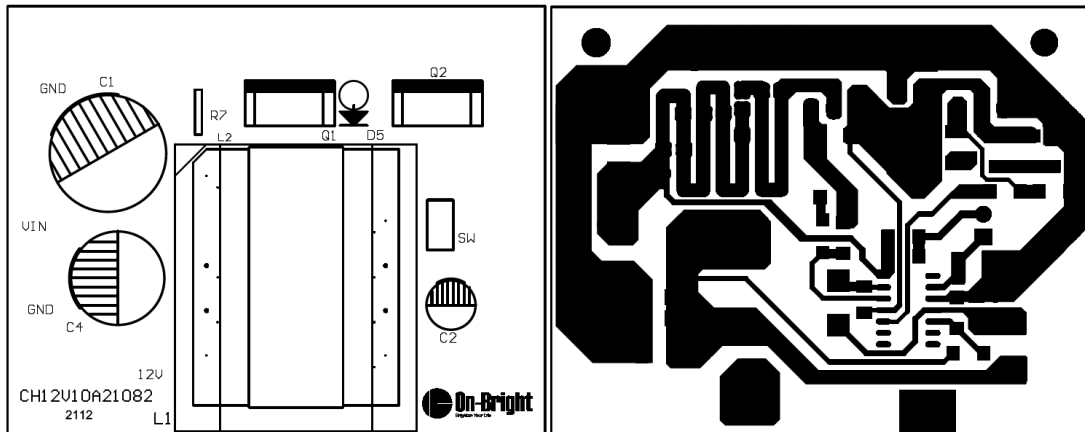
2.1. Schematic



2.2. Bill of Material

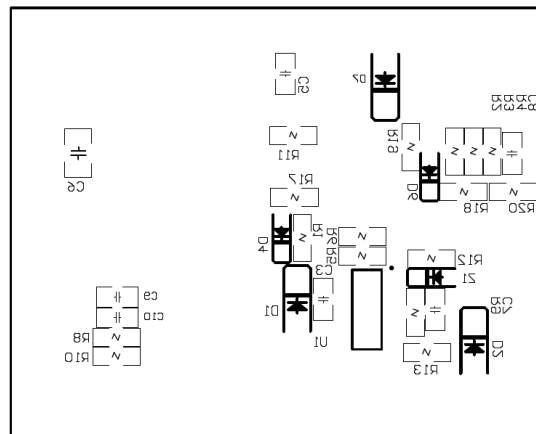
No.	Position	Description	Quantity	Remark
1	R1	RES SMD 1206 5.1R 5%	1	
2	R2,R3,R4	RES SMD 1206 33R 5%	3	
3	R5,R6	RES SMD 1206 180K 5%	2	
4	R8,R10	RES SMD 1206 1.5K 5%	2	
5	R9	RES SMD 1206 10K 1%	1	
6	R11,R12,R20	RES SMD 1206 10K 5%	3	
7	R13	RES SMD 1206 39K 1%	1	
8	R17	RES SMD 1206 0R 15%	1	
9	R18	RES SMD 1206 15R 15%	1	
10	C1	EC 100uF 160V	1	
11	C2	EC 10uF 50V	1	
12	C3	SMD 1206 56nF 50V	1	
13	C9	SMD 1206 1uF 50V	1	
14	C4	EC 1000uF 25V	1	
15	C6	SMD 1210 470nF 200V	1	
16	C7	SMD 1206 100nF 50V	1	
17	C8	SMD 1206 1nF1KV	1	
18	D1	SMA RS1M 1A/1KV	1	
19	D2,D4	SMD 1206 LL4148 0.15A/100V	2	
20	Q1	MOSFET FDP2532 150V 79A,16mohM,TO-220	1	
21	Q2	MOSFET FDP075N15A 150V 130A,7.5mohM,TO-220	1	
22	U1	OB21082CFP SO-14	1	
23	L1	Inductor EE30 30uH	1	
24	Z1	Zener, MMZJ 5.1,5.1V 500mW SOD-80C	1	
25	SW1	Pin header with pin jumper,2 pin,2.54mm	1	
26	heatsink	For Q1,Q2	1	
27	PCB	CH12V10A21082 2112	1	
	Total		34	

2.3. PCB Gerber File



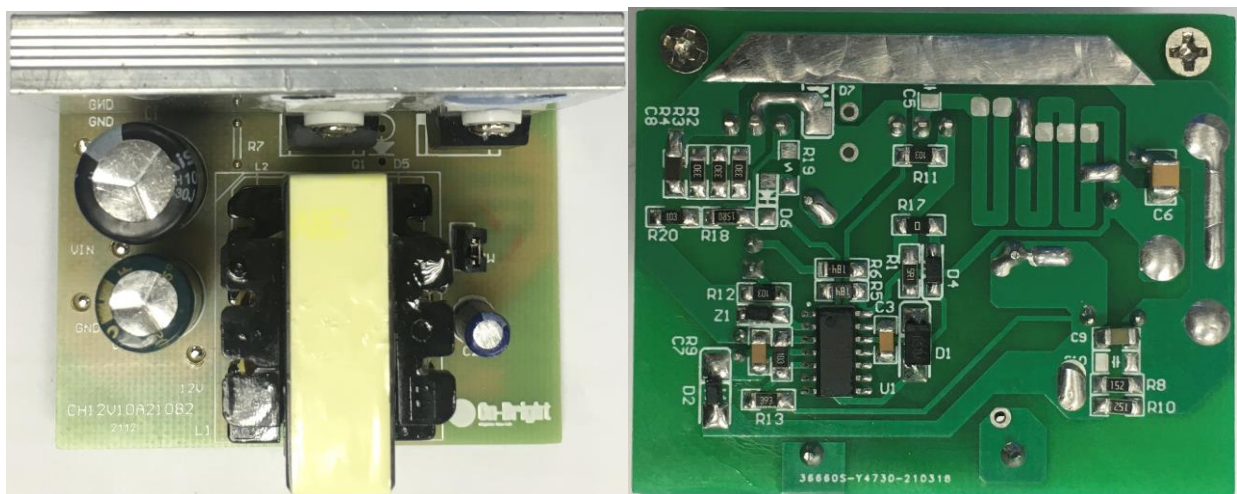
Top silkscreen

Bottom



Bottom silkscreen

2.4. Board Snapshot

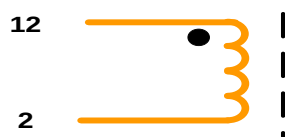


2.5. Inductor information

2.5.1 Inductor Specification

- 1) Bobbin: EE30 (6+6Pin)
- 2) Core material: PC40 (TDK).
- 3) $L(5-4) = 30\mu H \pm 5\%$ (10KHz, 1V, 25 °C)
- 4) cut pin1, pin3, pin4, pin5, pin8, pin9, pin10, pin11

2.5.2 Wingding data



Winding	Material	Start	Turns	Finish
N ₁	Φ0.1 *150 2UEW	12	11.5	2

3. Performance Evaluation

3.1. Efficiency(@board end)

Input voltage	Load				Specification
	4.16A	5A	8.33A	10A	
36Vdc	95.74%	95.54%	94.7%	94%	>86%
60Vdc	95.06%	94.93%	94.28%	93.67%	
96Vdc	92.77%	93.31%	93%	92.5%	

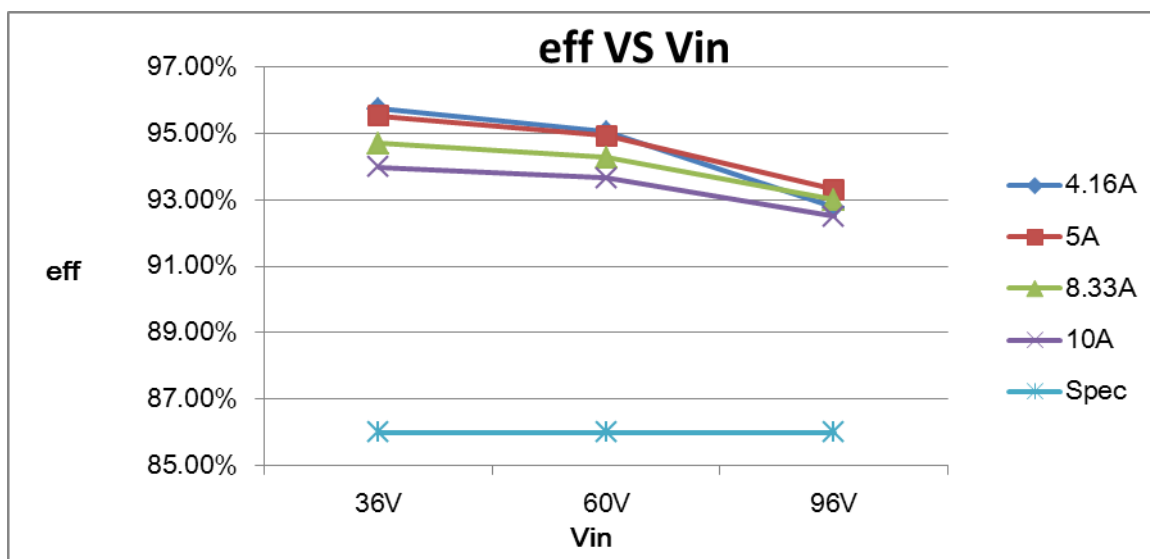


Fig. 1 Efficiency vs. Percent of Rated Output Power

3.2. Line Regulation & Load Regulation

Input voltage	No load	Full load	Specification
25Vdc	12.25V	12.15V	12V-12.5V
60Vdc	12.25V	12.15V	
96Vdc	12.24V	12.14V	
118Vdc	12.24V	12.14V	

3.3. Ripple & Noise

Input voltage	No load	Full load	Specification	Remark
25Vdc	213mV	193mV	<600mV	Fig. 2,3
60Vdc	199mV	146mV		
96Vdc	199mV	153mV		
118Vdc	213mV	173mV		Fig. 4,5

Note: Ripple& noise was measured at load end with probe cap, and bandwidth was limited to 20MHZ.

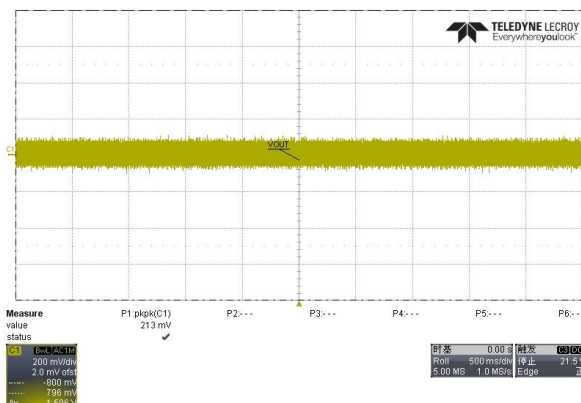


Fig. 2 Measured ripple& noise @25Vdc, no load.

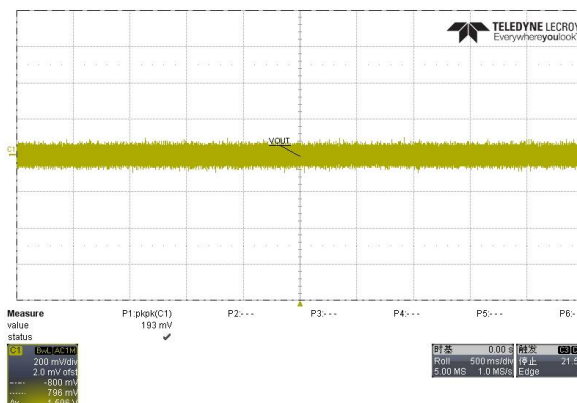


Fig.3 Measured ripple& noise @25Vdc, full load.

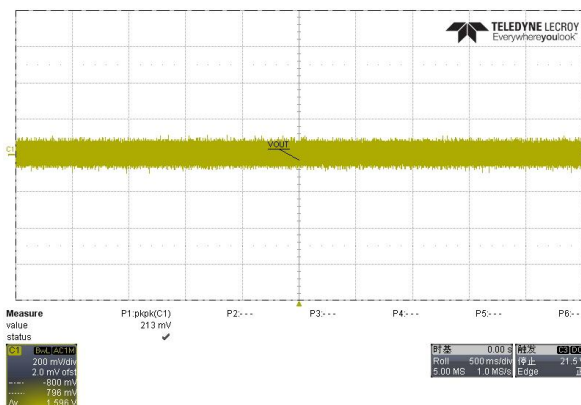


Fig.4 Measured ripple& noise @118Vdc, no load

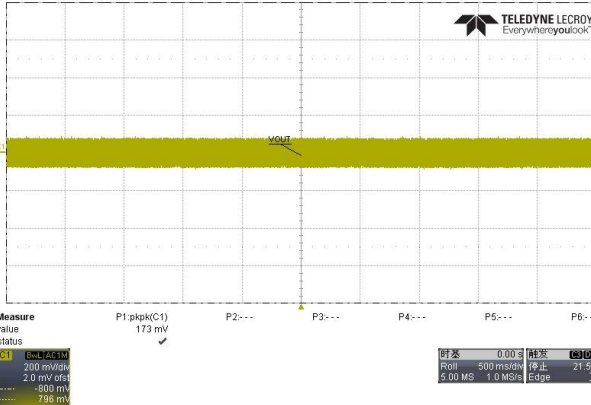


Fig.5 Measured ripple& noise @118Vdc, full load

3.4. Dynamic Test

A dynamic loading with low set at no load lasting for 50ms and high set at 10A load lasting for 50ms is added to output. The ramp is set at 0.25A/us at transient. Measurement was taken at board end(Same as R&N measurement)

Input	Output voltage		Remark
	V _{MAX} (V)	V _{MIN} (V)	
25Vdc	12.43	11.57	Fig.6
60Vdc	12.43	11.86	
96Vdc	12.42	11.87	
118Vdc	12.42	11.87	Fig.7

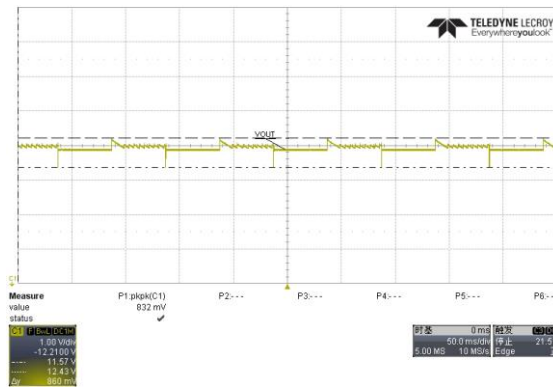


Fig.6 Output voltage under Dynamic test @ 25Vdc

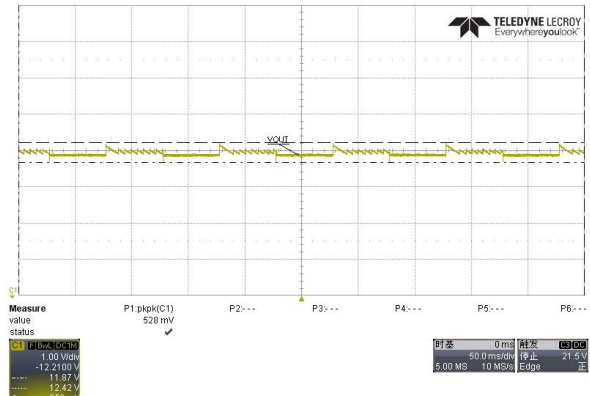


Fig.7 Output voltage under Dynamic test @ 118Vdc

3.5. Turn Off Delay

The IC is enabled when SW is on, and disabled when off, the system will shutdown about 20 seconds later.

Input	No load	Full load	Remark
25Vdc	20.6S	20.6S	Fig.8 Fig.9
118Vdc	20.6S	20.6S	Fig.10 Fig.11

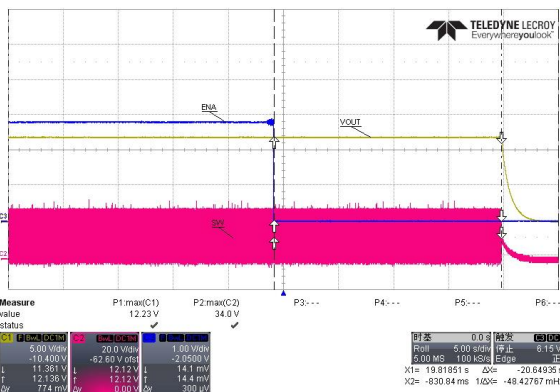


Fig.8 Disable, V_{DS1} , V_{ena} , V_o , V_{cc} @25Vdc, no load

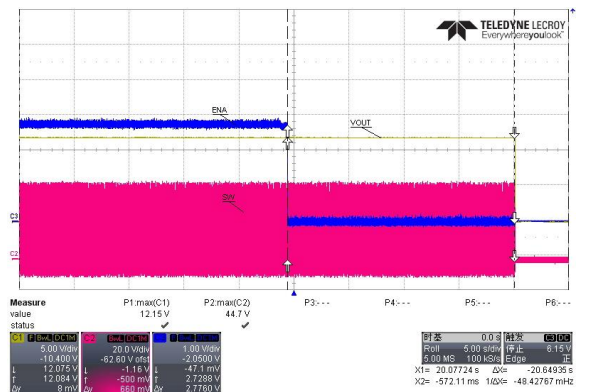


Fig.9 Disable, V_{DS1} , V_{ena} , V_o , V_{cc} @25Vdc, full load

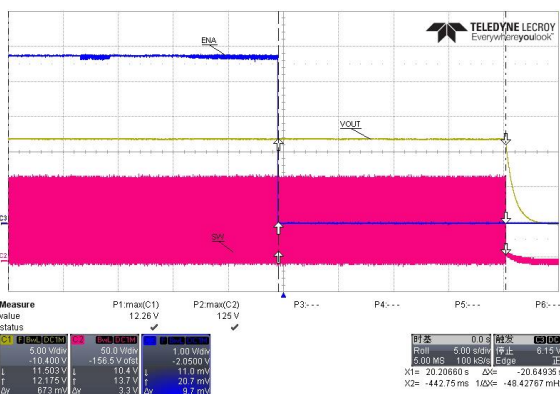


Fig.10 Disable, V_{DS1} , V_{ena} , V_o , V_{cc} @118Vdc, no load

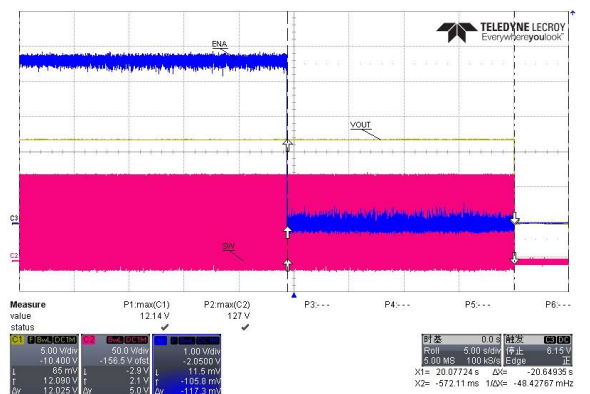


Fig.11 Disable, V_{DS1} , V_{ena} , V_o , V_{cc} @118Vdc, full load

4. Protection

4.1. Short Circuit Protection

The system is protected during output short circuit condition and recovered 10 times and then latched. Latch released when IC reenabled or the input voltage drops to below $V_{in\ UVP}$.

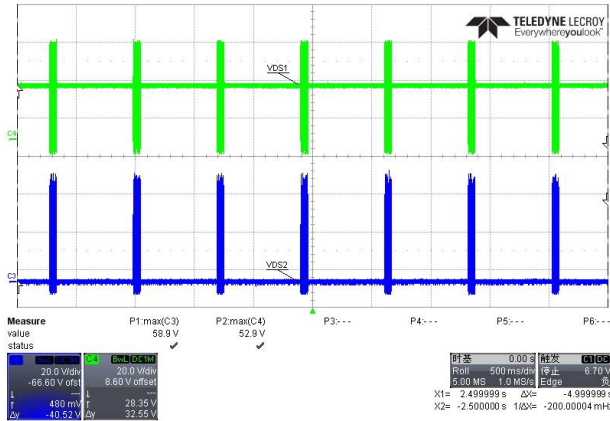


Fig.12 Output short, V_{DS1} , V_{DS2} @25Vdc

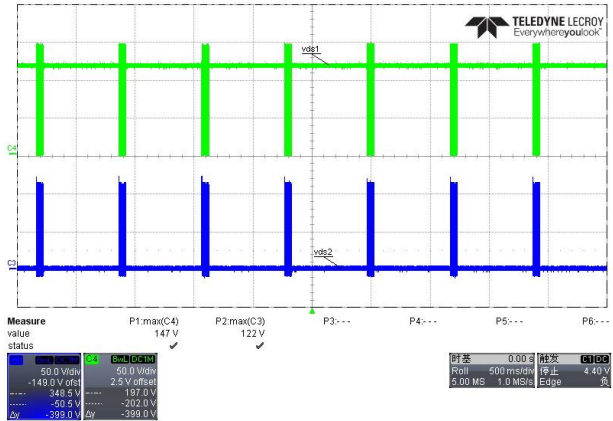


Fig.13 Output short, V_{DS1} , V_{DS2} @118Vdc

4.2. Over Current Protection

Input Voltage	25Vdc	48Vdc	72Vdc	96Vdc
OCP	15.5A	15.9A	15.9A	16.5A

4.3. Input Over Voltage Protection

		Test Result	Specification	Remark
Vin OVP	ON	126V	125V-133V	PASS
	OFF	121V	117V-125V	PASS

4.4. Input Under Voltage Protection

		Test Result	Specification	Remark
Vin UVP	ON	14.1V	13V-15V	PASS
	OFF	15.0V	14V-16V	PASS

4.5. Over Temperature Protection

		Test Result	Specification	Remark
OTP	ON	152°C	140°C-160°C	PASS
	OFF	133°C	125°C-145°C	PASS

5. Thermal Testing

Aluminum shell size 110x52x38mm³, ambient temperature 40°C, 120W load

Vin	Q1	Q2	core	coil	Spec
25VDC	65.4°C	68.7°C	95.6°C	100.9°C	115°C
118Vdc	103°C	87.7°C	108.9°C	114.9°C	

6. Other Waveforms

6.1. V_{DS1} , V_{DS2} & V_{CC} wave form @ no load / full load

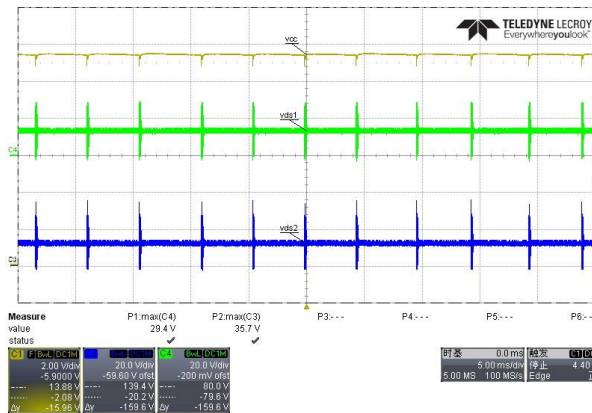


Fig. 14 V_{DS1} , V_{DS2} & V_{CC} waveform @ 25Vdc, no load

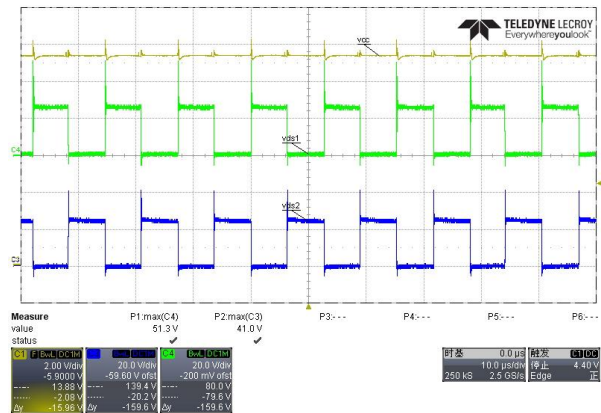


Fig. 15 V_{DS1} , V_{DS2} & V_{CC} waveform @ 25Vdc, full load

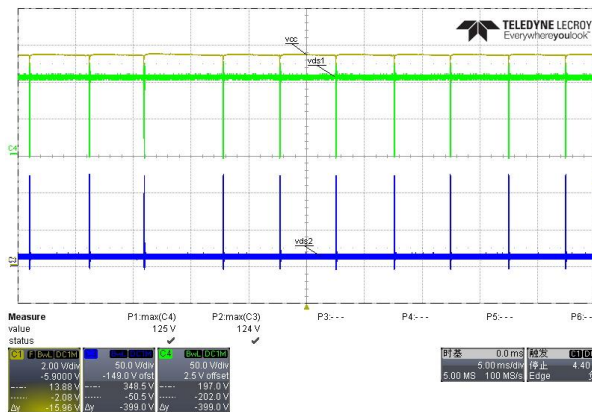


Fig. 16 V_{DS1} , V_{DS2} & V_{CC} waveform @ 118Vdc, no load

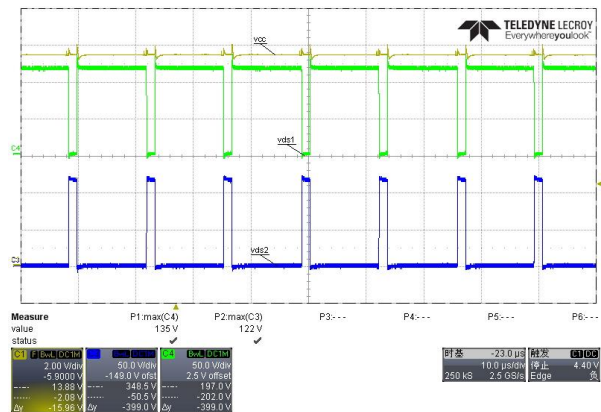


Fig. 17 V_{DS1} , V_{DS2} & V_{CC} waveform @ 118Vdc, full load

6.2. MOSFET V_{DS} waveform @ start / normal / output short

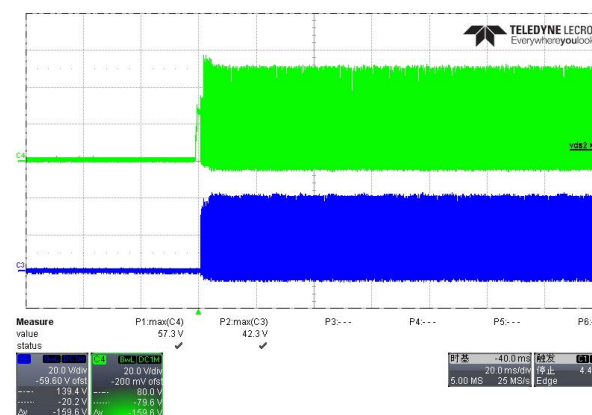


Fig. 18 Start, V_{DS1} , V_{DS2} @ 25Vdc, full load

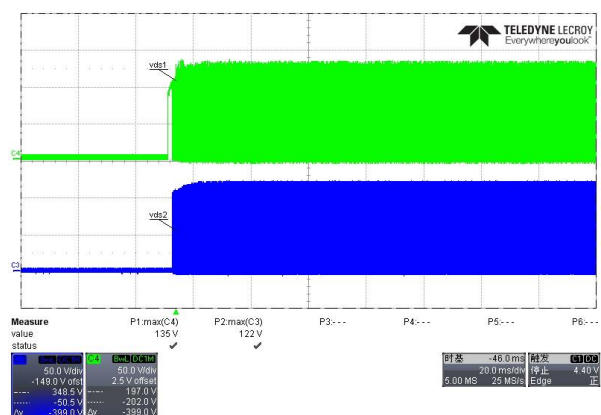


Fig. 19 Start, V_{DS1} , V_{DS2} @ 118Vdc, full load

 V_{DS1_MAX}, V_{DS2_MAX} @ Full load / Start / Output short

Input	$V_{DS1_MAX}(V)$	$V_{DS2_MAX}(V)$
118Vdc @ No load	125	124
118Vdc @ Full load	135	124
118Vdc @ Start	135	122
118Vdc @ Output short	147	122

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